

Expansion Connectors

The Odroid-c1 provides one 40-pin dual row expansion header “J2”. The location and pinout of these connectors is illustrated below.

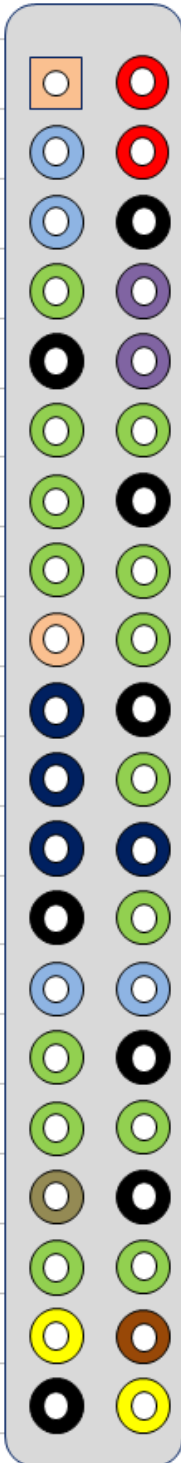
All signals on expansion headers are 3.3V except Analog input signal(1.8V).

Built-in pull-up/down resistor value is 60Kohm in the GPIOs.

J2 - 2x20 PINS

GPIO	wPi	Name	Alternative/ Driving Capability	Mode	V	PU/PD	PIN	PIN	PU/PD	V	Mode	Alternative/ Driving Capability	Name	wPi	GPIO
-	-	3.3V	-	-	-	-	1	2	-	-	-	-	5.0V	-	-
74	-	I2CA_SDA	-	IN	1	-	3	4	-	-	-	-	5.0V	-	-
75	-	I2CA_SCL	-	IN	1	-	5	6	-	-	-	-	GND	-	-
83	7	GPIOY.3	-/2mA	IN	0	P/U	7	8	P/U	1	ALT1	-	GPIOX.16	-	113
-	-	GND	-	-	-	-	9	10	P/U	1	ALT1	-	GPIOX.17	-	114
88	0	GPIOY.8	-/3mA	IN	1	P/U	11	12	P/U	0	IN	-/2mA	GPIOY.7	1	87
116	2	GPIOX.19	-/2mA	IN	1	P/U	13	14	-	-	-	-	GND	-	-
115	3	GPIOX.18	-/2mA	IN	0	P/D	15	16	P/U	1	IN	-/3mA	GPIOX.7	4	104
-	-	3.3V	-	-	-	-	17	18	P/U	1	IN	-/3mA	GPIOX.5	5	102
107	12	GPIOX.10	PWM1/2mA	IN	1	P/U	19	20	-	-	-	-	GND	-	-
106	13	GPIOX.9	-/3mA	IN	1	P/U	21	22	P/U	1	IN	-/3mA	GPIOX.6	6	103
105	14	GPIOX.8	-/4mA	IN	1	P/U	23	24	P/D	0	IN	-/2mA	GPIOX.20	10	117
-	-	GND	-	-	-	-	25	26	P/U	1	IN	-	GPIOX.21	11	118
76	-	I2CB_SDA	-	IN	1	-	27	28	-	1	IN	-	I2CB_SCL	-	77
101	21	GPIOX.4	-/3mA	IN	1	P/U	29	30	-	-	-	-	GND	-	-
100	22	GPIOX.3	-/3mA	IN	1	P/U	31	32	P/U	1	IN	-/3mA	GPIOX.2	26	99
108	23	GPIOX.11	PWM0/3mA	IN	0	P/D	33	34	-	-	-	-	GND	-	-
97	24	GPIOX.0	-/3mA	IN	1	P/U	35	36	P/U	1	IN	-/3mA	GPIOX.1	27	98
-	-	ADC.AIN0	10bit ADC#1(0~1.8V)	-	-	-	37	38	-	-	-	Output!	1.8V REF	-	-
-	-	GND	-	-	-	-	39	40	-	-	-	10bit ADC#0 (0~1.8V)	ADC.AIN1	-	-

ODROID C1/C1+ (J2 Header)

<i>WiringPi GPIO#</i>	<i>NAME(GPIO#)</i>				<i>NAME(GPIO#)</i>	<i>WiringPi GPIO#</i>
	3.3 V Power	1		2	5.0 V Power	
	I2CA_SDA (#74)	3		4	5,0 V Power	
	I2CA_SCL (#75)	5		6	Ground	
7	GPIO (#83)	7		8	TXD1 (#113)	
	Ground	9		10	RXD1 (#114)	
0	GPIO (#88)	11		12	GPIO (#87)	1
2	GPIO (#116)	13		14	Ground	
3	GPIO (#115)	15		16	GPIO (#104)	4
	3.3V Power	17		18	GPIO (#102)	5
12	MOSI_PWM1 (#107)	19		20	Ground	
13	MISO (#106)	21		22	GPIO (#103)	6
14	SPI_SCLK (#105)	23		24	GPIO (#117)	10
	Ground	25		26	GPIO (#118)	11
	I2CB_SDA (#76)	27		28	I2CB_SCL (#77)	
21	GPIO (#101)	29		30	Ground	
22	GPIO (#100)	31		32	GPIO (#99)	26
23	PWM0 (#108)	33		34	Ground	
24	GPIO (#97)	35		36	GPIO (#98)	27
AIN1	ADC.AIN1 (ADC#1)	37		38	1.8 V Power	
	Ground	39		40	ADC.AIN0 (ADC#0)	AIN0

Attention! The WiringPi GPIO pin numbering used in this diagram is intended for use with WiringPi. The raw chipset GPIO pin numbering is "(#number)"

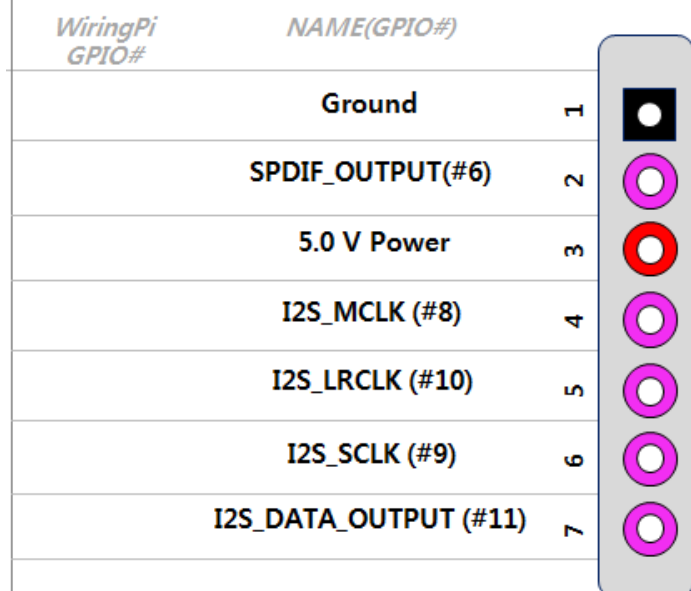
[Http://www.hardkernel.com](http://www.hardkernel.com)

J7 - 1x7 PINS

This I2S expansion connector exists only on the C1+

GPIO	Name	Alternative/ Driving Capability	Mode	V	PU/PD	PIN
-	GND	-	-	-	-	1
6	GPIOAO.6	I2S Data Input/2mA	IN	0	-	2
-	5.0V	-	-	-	-	3
8	GPIOAO.8	I2S MCLK/2mA	ALT2	0	P/U	4
10	GPIOAO.10	I2S LRCLK/2mA	ALT2	0	P/U	5
9	GPIOAO.9	I2S SCLK/2mA	ALT2	0	P/U	6
11	GPIOAO.11	I2S Data output/2mA	ALT2	0	P/U	7

ODROID C1+ (J7 Header)



Attention! The WiringPi GPIO pin numbering used in this diagram is intended for use with WiringPi. The raw chipset GPIO pin numbering is "(#number)"

[Http://www.hardkernel.com](http://www.hardkernel.com)

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Last update: 2017/09/27 10:50



